REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1, 3-26, 34, 36, 65, and 66 were pending and rejected. In this response, claims 1, 4, 7, 12, 18, 22, 34, 65 and 66 have been amended to particularly point out and distinctly claim, in full, clear, concise, and exact terms, the subject matter which Applicants regard as their invention. No new matter has been added.

Rejections under 35 U.S.C. § 103

Claims 1-2, 7-10, 18-21, and 34-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, US 6,868,504 (hereinafter "Lin") in view of Lo et al., US Publication 2003/0102894 (hereinafter "Lo").

Claim 1, as amended, recites:

> 1. A programmable delay cell comprising:
> a first capacitor coupled to a low supply rail;
> a conductor coupled to an output of said programmable delay cell; and
> **three or more pass gates coupled in parallel to each other**, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and **a second terminal of the each of the three or more pass gates is coupled to the same first capacitor**, wherein impedance of each of said pass gates is to be controlled by an independent control signal, such that **combined impedance of said pass gates is controlled by at least three control signals**. (Emphasis added)

Applicants submit that Lin and Lo fail to disclose at least "three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the same first capacitor" and "a combined impedance of said pass gates are controlled by at least three control signals" as required in claim 1 (emphasis added).

Referring to Lin, Lin discloses a delay line for use in phase locked loop and delay locked loop circuits (Figure 3a). Lin describes that load can be adjusted through operation of switches 47-54 (column 3, line 67 to column 4, line 17). Claim 1 requires the second terminal of each of the pass gates coupled directly to a same capacitor. In Lin, each the switches 47-54 is connected to a separate capacitor. For example, switch 47 is connected to capacitor 56; switch 48 is connected to capacitor 57; etc. Switches 47-54 are **not** connected to one same capacitor as required in Claim 1.

Therefore, Lin fails to teach at least the limitation "three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the same first capacitor" as required in claim 1. Figure 3 in Lin is shown below for reference purpose.

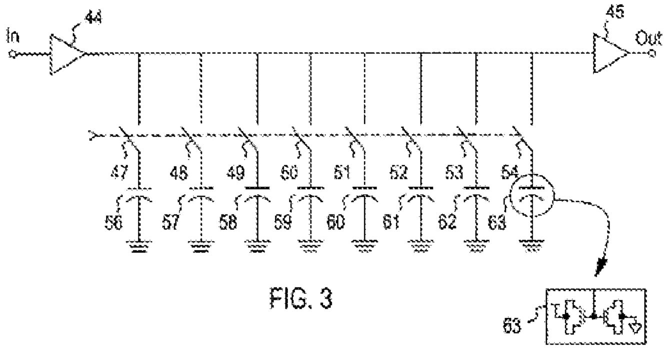

FIG. 3

Figure 3 in Lin (as indicated in the Office Action)

Moreover, Lin fails to disclose "three or more pass gates coupled in parallel to each other". There is no mention of pass gates and control signals in Lin's disclosure. Lo is relied on to disclose the limitation. Lo discloses replacing each transistor with only a pass gate to perform the intended function as indicated in the Office Action in the comparison of Figure 7 and Figure 14 in Lo. Lo's circuit fails to teach "three or more pass gates coupled in parallel to each other". There is also no mention of combined impendence value in Lin and Lo.

Moreover, the control signal of both pass gates (Lo, Figure 14, pass gate 3-8; pass gate 4-9) is derived from a same control signal such that the pass gate function as one buffer as intended (Lo, Figure 14). Therefore, Lo also fails to disclose "wherein impedance of each of said pass gates is to be controlled by an independent control signal, such that a combined impedance of said pass gates is controlled by at least three control signals". Applicants also submit that Lo's pass gates must operate in a complementary manner otherwise Lo's circuit would be rendered inoperable. Lin and Lo, even if combined, would still fail to teach all the elements of claim 1.

Furthermore, Lo discloses using pass gates as a buffer, but fails to teach controlling impedance of each of the pass gates. There is also no mention of combined impedance in both Lin and Lo. Thus, one skilled in the art would not look into Lo for controlling impedance of each of pass gates. Therefore, it is also not obvious to combine Lin and Lo. At least for the foregoing reasons, Applicants submit that claim 1 is not obvious over Lin and Lo. Applicants respectfully request that the rejection for claim 1 under 103(a) be withdrawn.

Claims 7, 18, and 34, as amended, require "three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to the same first capacitor". Applicants would like to submit that Lin and Lo fail to teach at least this limitation. Detailed remarks with respect to claim 1 are incorporated herein by reference.

At least for the foregoing reasons, Applicants believe that claims 7, 18, and 34 are not obvious over Lin and Lo. Claims 8-10 and 19-21, depending from claims 7 and 18 respectively, are also allowable for at least the same reason. Applicants respectfully request that the rejections for the claims be withdrawn.

Claim 3 and 36 are rejected under 35 U.S.C. 103(a) as being obvious over Lin in view of Lo and Reddy, US 5,847,617 (hereinafter "Reddy"). Claim 3 and 36, depending from claims 1 and 34 respectively, are not obvious over Lin and Lo. As set forth above, Lin and Lo fail to disclose the limitations as explained above. Reddy does not cure the deficiency of Lin and Lo. Applicants respectfully request that the rejections for the claims be withdrawn.

Claims 4-6, 12-16, and 66 are rejected under 35 U.S.C. 103(a) as being obvious over Lin in view of Lo and Reddy. Claim 4, as amended, recites:

> 4. A programmable delay cell comprising:
> a conductor coupled to an output of said programmable delay cell;
> a switch transistor coupled to the conductor;
> **three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to one same capacitor coupled to a low supply rail**; and
> a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor such that a drain terminal of the switch transistor does not reside between the source terminal of the switch transistor and the variable impedance transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal. (Emphasis added)

Applicants would like to submit that Lin, Lo, and Reddy fail to disclose at least "three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to one same capacitor coupled to a low supply rail" (emphasis added) as required in claim 4. The rejection in the Office Action is moot in view of the amended claim. Detailed remarks with respect to claim 1 are incorporated herein by reference.

Both claims 12 and 22 require "three or more pass gates coupled in parallel to each other, wherein a first terminal of each of the three or more pass gates is coupled to the conductor and a second terminal of the each of the three or more pass gates is coupled to one same capacitor coupled to a low supply rail" (emphasis added). Applicants would like to submit that Lin, Lo, and Reddy fail to disclose at least this limitation. Detailed remarks with respect to claim 1 are incorporated herein by reference.

At least for the foregoing reasons, Applicants believe that claim 4, 12, 22 are not obvious over Lin, Lo, and Reddy. Claims 5-6, 13-16, and 23-26 depending from claims 4, 12, and 22 are also allowable for at least the same reason. Applicants respectfully request that the rejections for the claims be withdrawn.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Lo, and Ota US 6,868,504 (hereinafter "Ota"). Claim 11 depends from claim 7 which is not obvious over Lin, Lo, and Reddy as explained above. Ota fails to cure the deficiency of Lin and Lo with respect to claim 7. Applicants respectfully request that the rejection for the claim be withdrawn.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Lo, Reddy, and Ota. Claim 17 depends from claim 12 which is allowable over Lin, Lo, and Reddy. Ota fails to cure the deficiency of Lin and Reddy with respect to claim 12. Applicants believe that claim 17 is not obvious over Lin, Reddy, and Ota. Applicants respectfully request that the rejection for the claim be withdrawn.

Amended Claims

Applicants have amended dependent claims 65-66 which depend from claim 1. In view of the foregoing reasons, independent claims 1 is allowable and therefore the dependent claims 65-66 are also allowable over the cited references.

Claim 65 requires "wherein the second terminal of the each of the three or more pass gates is coupled directly to a node which is then coupled directly to the first capacitor, wherein no other capacitor is disposed between the second terminal and the node, wherein only one capacitor is disposed between the first conductor and the low supply rail". Claim 66 requires "wherein the three or more pass gates are in parallel as the first terminal of each of the pass gates is coupled directly to the first conductor, wherein the second terminal of each of the pass gates is coupled directly to a same node without any intermediate component". The cited references fail to teach the limitations as set forth in the claims above. In particular, Lin requires that each of the switches is connected to a separate capacitor. **The switch is not coupled directly to a same capacitor** (Lin, figure 3).

Lo discloses replacing each transistor with only a pass gate to perform the intended function as indicated in the Office Action in the comparison of Figure 7 and Figure 14 in Lo. There is also no mention of combined impendence value in Lin and Lo.

Therefore, at least for the foregoing reasons, Applicants submit that claims 65-66 are allowable over the cited references. Applicants respectfully request the allowance for claims 65-66.

CONCLUSION

In view of the foregoing, Applicants respectfully submit the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (503) 439-8778.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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